What is claimed is:

1. A semiconductor device which comprises external interface terminals and processing circuits, and which is fed with an operating power source when detachably set in a host equipment, wherein:

said external interface terminals include power source feeding terminals, an extraction detecting terminal, and other terminals;

said power source feeding terminals are long enough to keep touching corresponding terminals of the host equipment for, at least, a predetermined time period since separation of said extraction detecting terminal from a corresponding terminal of the host equipment;

said power source feeding terminals are formed to be longer in an extraction direction than said extraction detecting terminal;

said processing circuits include an interface control circuit which is connected to said external interface terminals, and a rewritable nonvolatile memory which is controlled by said interface control circuit;

said nonvolatile memory stores information on the basis of a difference of threshold voltages of memory cells; and

said interface control circuit causes said nonvolatile memory midway of a rewrite process to complete a predetermined process, before cutoff of the power source after the separation

of said extraction detecting terminal from the corresponding terminal of the host equipment.

2. A semiconductor device according to claim 1, wherein the predetermined process is a process in which the threshold voltages of said memory cells are uniformalized into a predetermined threshold voltage distribution, for a storage area midway of a threshold voltage initialization process.

3. A semiconductor device according to claim 1, wherein the predetermined process is a process which completes storage of information in a management area which is required for recognition of a storage area.

4. A semiconductor device according to claim 1, wherein the predetermined process is a process which completes midway storage of information after a threshold voltage initialization process.

5. A semiconductor device according to claim 1, wherein said power source feeding terminals are made longer than said extraction detecting terminal, also on a side opposite to the extraction direction, and a length which said power source feeding terminals protrude on the opposite side to the extraction direction, beyond said extraction detecting terminal, is smaller than a length which they protrude in the extraction direction.

6. A semiconductor device according to claim 1, wherein said interface control circuit instructs said nonvolatile

memory to execute the predetermined process, by detecting the separation of said extraction detecting terminal.

7. A semiconductor device according to claim 1, wherein said interface control circuit instructs said nonvolatile memory to execute the predetermined process, in response to a command which is supplied from the host equipment when said extraction detecting terminal has been separated from the corresponding terminal of the host equipment.

8. A semiconductor device which comprises external interface terminals and processing circuits, and which is fed with an operating power source when detachably set in a host equipment, wherein:

said external interface terminals include power source feeding terminals, an extraction detecting terminal, and other terminals;

said power source feeding terminals are long enough to touch corresponding terminals of the host equipment for, at least, 1.0 millisecond since separation of said extraction detecting terminal from a corresponding terminal of the host equipment, with respect to an extraction speed of 2.5 meters/second;

said processing circuits include an interface control circuit which is connected to said external interface terminals, and a rewritable nonvolatile memory which is controlled by said interface control circuit;

said nonvolatile memory stores information on the basis of a difference of threshold voltages of memory cells; and

said interface control circuit causes said nonvolatile memory midway of a rewrite process to complete a predetermined process, before cutoff of the power source after the separation of said extraction detecting terminal from the corresponding terminal of the host equipment.

9. A semiconductor device according to claim 8, wherein the predetermined process is a process in which the threshold voltages of said memory cells are uniformalized into a predetermined threshold voltage distribution, for a storage area midway of a threshold voltage initialization process.

10. A semiconductor device according to claim 8, wherein the predetermined process is a process which completes storage of information in a management area which is required for recognition of a storage area.

11. A semiconductor device according to claim 8, wherein the predetermined process is a process which completes midway storage of information after a threshold voltage initialization process.

12. A semiconductor device according to claim 8, wherein said power source feeding terminals are formed to be longer in an extraction direction than said extraction detecting terminal.

13. A semiconductor device according to claim 12,

wherein said power source feeding terminals are made longer than said extraction detecting terminal, also on a side opposite to the extraction direction, and a length which said power source feeding terminals protrude on the opposite side to the extraction direction, beyond said extraction detecting terminal, is smaller than a length which they protrude in the extraction direction.

14. A semiconductor device according to claim 8, wherein said interface control circuit instructs said nonvolatile memory to execute the predetermined process, by detecting the separation of said extraction detecting terminal.

15. A semiconductor device according to claim 8, wherein said interface control circuit instructs said nonvolatile memory to execute the predetermined process, in response to a command which is supplied from the host equipment when said extraction detecting terminal has been separated from the corresponding terminal of the host equipment.

16. A semiconductor device which comprises external interface terminals and processing circuits, and which is fed with an operating power source when detachably set in a host equipment, wherein:

said external interface terminals are arranged in two rows in a direction crossing an extraction direction, and they include power source feeding terminals, an extraction detecting terminal, and other terminals;

said power source feeding terminals are long so as to extend from the first row over to the second row;

said processing circuits include an interface control circuit which is connected to said external interface terminals, and a rewritable nonvolatile memory which is controlled by said interface control circuit;

said nonvolatile memory stores information on the basis of a difference of threshold voltages of memory cells; and

said interface control circuit causes said nonvolatile memory midway of a rewrite process to complete a predetermined process, before cutoff of the power source after separation of said extraction detecting terminal from a corresponding terminal of the host equipment.

17. A semiconductor device according to claim 16, wherein the predetermined process is a process in which the threshold voltages of said memory cells are uniformalized into a predetermined threshold voltage distribution, for a storage area midway of a threshold voltage initialization process.

18. A semiconductor device according to claim 16, wherein the predetermined process is a process which completes storage of information in a management area which is required for recognition of a storage area.

19. A semiconductor device according to claim 16, wherein the predetermined process is a process which completes midway storage of information after a threshold voltage

initialization process.

20. A semiconductor device according to claim 16, wherein said interface control circuit instructs said nonvolatile memory to execute the predetermined process, by detecting the separation of said extraction detecting terminal.

21. A semiconductor device according to claim 16, wherein said interface control circuit instructs said nonvolatile memory to execute the predetermined process, in response to a command which is supplied from the host equipment when said extraction detecting terminal has been separated from the corresponding terminal of the host equipment.

22. A semiconductor device which comprises external interface terminals and processing circuits, and which is fed with an operating power source when detachably set in a host equipment, wherein:

said external interface terminals include power source feeding terminals, an extraction detecting terminal, and other terminals;

said power source feeding terminals are long enough to keep touching corresponding terminals of the host equipment for, at least, a predetermined time period since separation of said extraction detecting terminal from a corresponding terminal of the host equipment;

said power source feeding terminals are formed to be

longer in an extraction direction than said extraction detecting terminal; and

said processing circuits complete a predetermined necessary process before cutoff of the power source, when said extraction detecting terminal has been separated from the corresponding terminal of the host equipment.

23. A semiconductor device which comprises external interface terminals and processing circuits, and which is fed with an operating power source when detachably set in a host equipment, wherein:

said external interface terminals include power source feeding terminals, an extraction detecting terminal, and other terminals;

said power source feeding terminals are long enough to touch corresponding terminals of the host equipment for, at least, 1.0 millisecond since separation of said extraction detecting terminal from a corresponding terminal of the host equipment, with respect to an extraction speed of 2.5 meters/second; and

said processing circuits complete a predetermined necessary process before cutoff of the power source, when said extraction detecting terminal has been separated from the corresponding terminal of the host equipment.

24. A semiconductor device which comprises external interface terminals and processing circuits, and which is fed

with an operating power source when detachably set in a host equipment, wherein:

said external interface terminals are arranged in two rows in a direction crossing an extraction direction, and they include power source feeding terminals, an extraction detecting terminal, and other terminals;

said power source feeding terminals are long so as to extend from the first row over to the second row, said extraction detecting terminal is arranged at the first row, and said other terminals are arranged at the first and second rows; and

said processing circuits complete a predetermined necessary process before cutoff of the power source, when said extraction detecting terminal has been separated from a corresponding terminal of the host equipment.